

Designing ASICs With UAHPL

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Summary

Discussed the progress made in putting together a UAHPL based design automation system using software tools developed locally and in U.S. universities. The UAHPL language is used as the front-end specification medium because of its close relation to hardware implementation issues. The system is modular and technology independent so that future extensions and specific implementation issues can be added and modified. The work carried out so far has targeted semicustom design and standard cell methodologies. The front-end of the system, up to the netlist, is independent of technology and architecture. The output of this stage can be conveniently mapped to programmable devices (PLDs) and field programmable gate arrays (FPGAs)

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